凌陽科技
SUNPLUS

SPC500A1

512KB SOUND CONTROLLER

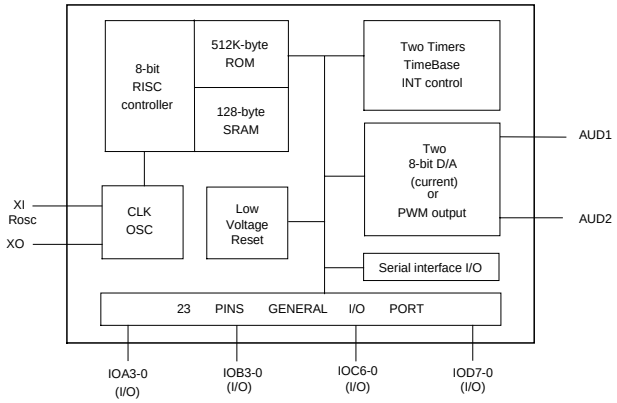
GENERAL DESCRIPTION

The SPC500A1 is a CPU based two-channel speech/melody synthesizer including CMOS 8-bit microprocessor with 69 instructions, 512K-byte ROM for speech and melody data (Speech is compressed by a 4-bit ADPCM with approx. 120 sec speech duration @ 7KHz sampling rate) and 128-byte working SRAM. It includes two Timer/Counters, 23 Software Selectable I/Os, two 8-bit current outputs D/A (or one PWM audio output) and serial interface I/O port. It provides Multi-Duty-Cycle output for remote control purposes. For audio processing, melody and speech can be mixed into one output. It operates over a wide voltage range of 2.4V - 5.5V and includes Low Voltage Reset function. The Low Voltage Reset automatically resets when the working voltage is less than 2.2V. Volume control is provided. In addition, the SPC500A1 has a Clock Stop mode for power savings. The power savings mode saves the RAM contents, but freezes the oscillator, causing all other chip functions to be inoperative. The Max. CPU clock frequency is 8.0MHz. It has an Instruction Cycle Rate of 2 clock cycles (min.) – 6 clock cycles (max.). The SPC500A1 includes, not only the latest technology, but also the full commitment and technical support of Sunplus.

FEATURES

- 8-bit microprocessor
- **Provides 512K-byte ROM for program and audio data**
- **128-byte working SRAM**
- Software-based audio processing
- Wide operating voltage: 2.4V – 3.4V@ 5.0MHz
  3.6V – 5.5V@ 8.0MHz
- Supports Crystal Resonator or Rosc (with Mask option)
- Max. CPU clock: 5.0MHz@3V, 8.0MHz@5V
- Two 12-bit timer/counters
- Standby mode (Clock Stop mode) for power savings. Max. 2μA @ 5V
- 500ns instruction cycle time @ 4.0MHz CPU clock
- 6 INT sources
- Key wake -up function
- **Provides 23 general I/Os**
- **Serial interface I/O**
- **Approx. 120 sec speech @ 7KHz sampling rate with ADPCM**
- **One PWM audio output (single speaker)**
- **Two DA output**
- **Multi-duty cycle mode**
- **Low Voltage Reset**
- **Volume control function**

BLOCK DIAGRAM



APPLICATION FIELD

- Intelligent education toys
  Ex. Pattern to voice (animal, car, color, etc.)
  Spelling (English or Chinese)
  Math
- High end toy controller
- Talking instrument controller
- General speech synthesizer
- Industrial controller

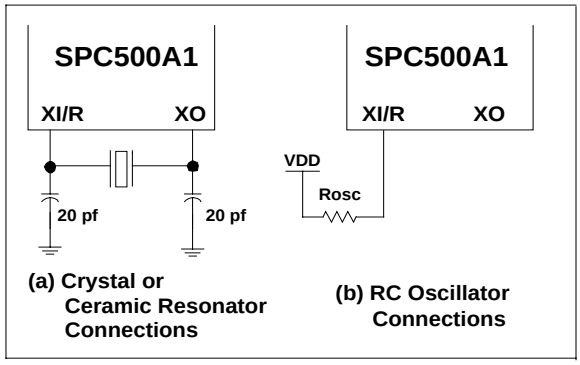
FUNCTION DESCRIPTIONS

■ CPU

The 8-bit microprocessor of SPC500A1 is a high performance processor equipped with Accumulator, Program Counter, X Register, Stack pointer and Processor Status Register (this is the same as the 6502 instruction structure). SPC500A1 is able to perform with 8.0MHz (max.) depending on the application specifications.

■ OSCILLATOR

The SPC500A1 supports AT-cut parallel resonant oscillated Crystal / Resonator or RC Oscillator or external clock sources by mask option (select one from those three types). The design of application circuit should follow the vendors' specifications or recommendations. The diagrams listed below are typical X'TAL/ROSC circuits for most applications:



■ MASK OPTION

The SPC500A1 has the following mask option:

- Supports Crystal Resonator or Rosc (with mask option).

■ ROM AREA

The SPC500A1 provides a 512K-byte ROM that can be defined as the program area, audio data area, or both. To access ROM, users should program the BANK SELECT Register, choose bank, and access address to fetch data.

■ RAM AREA

The SPC500A1 total RAM consists of 128 bytes (including Stack) at locations from $80 through $FF.

■ VOLUME CONTROL FUNCTION

The SPC500A1 contains a volume control function that provides an 8-step volume controller to control current D/A output. A volume control function selector (Enable/Disable) register and controller register is provided.

■ MAP OF MEMORY AND I/Os

*I/O PORT:

- PORT IOA $0004
  IOB $0005

- I/O CONFIG $0000
  $0001

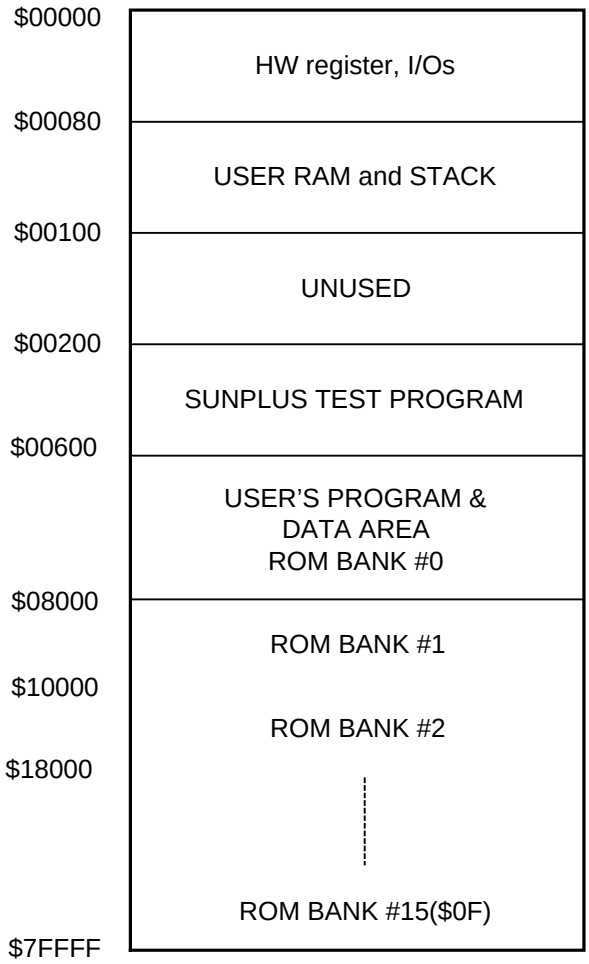
*NMI SOURCE:

- INTA (from TIMER A)

*INT SOURCE:

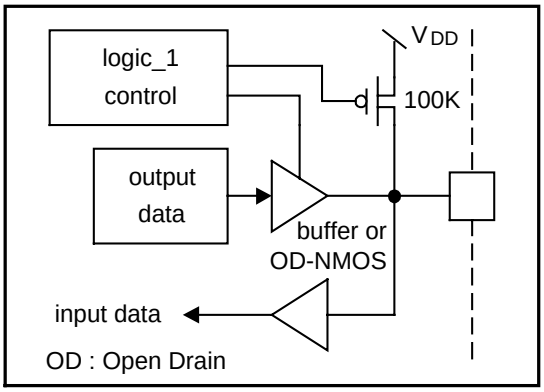
- INTA (from TIMER A)
- INTB (from TIMER B)
- CPU CLK / 1024
- CPU CLK / 8192
- CPU CLK / 65536
- EXT INT

*MEMORY MAP (From ROM view)

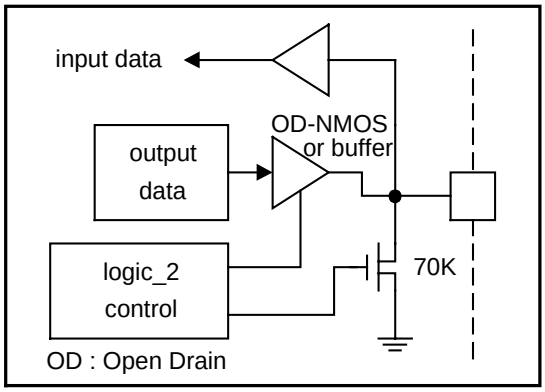


■ I/O PORT CONFIGURATIONS*

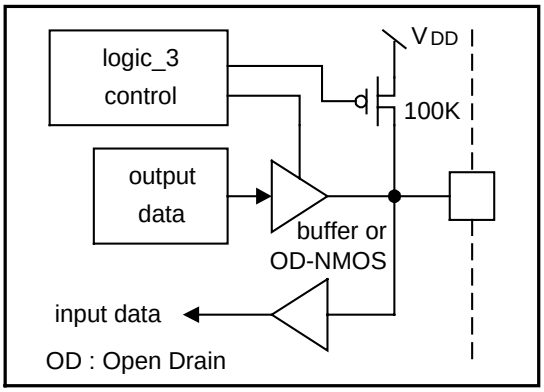
Input/Output IOA port : IOA3 - IOA0



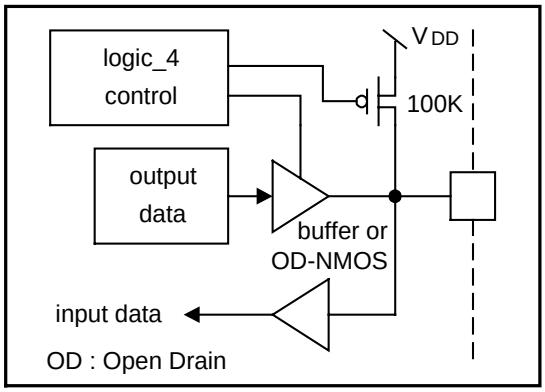
Input/Output IOB port : IOB3 -IOB0



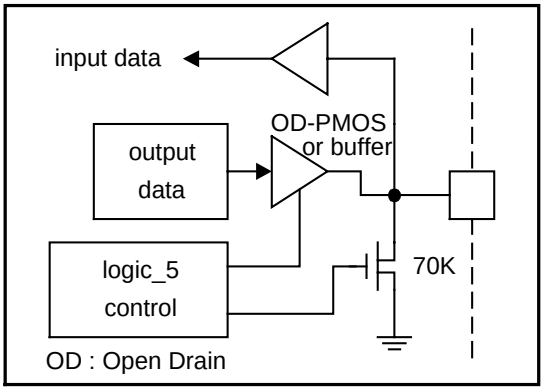
Input/Output IOC port : IOC3 - IOC0



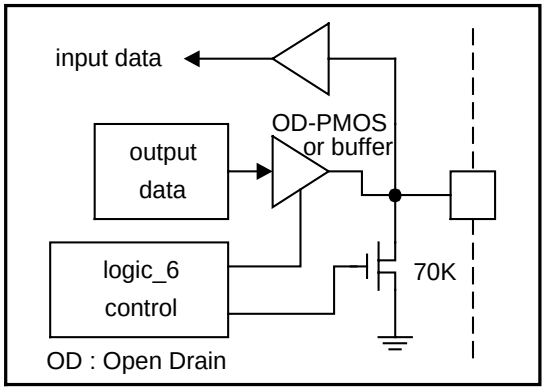
Input/Output IOC port : IOC6 - IOC4



Input/Output IOD port : IOD3 - IOD0



Input/Output IOD port : IOD7 - IOD4



*Values shown are for VDD = 5.0V test conditions only.

■ POWER SAVINGS MODE

The SPC500A1 provides a power savings mode (Standby mode) for those applications that require very low stand-by current. To enter standby mode, the Wake-Up Register should be enabled and then stop the CPU clock by writing the STOP CLOCK Register. The CPU will then go to the stand-by mode. In such a mode, RAM and I/Os will remain in their previous states until being awakened. Port IOD7-0 is the only wake-up source in the SPC500A1. After the SPC500A1 is awakened, the internal CPU will go to the RESET State (Tw ≧ 65536 x T1) and then continue processing the program. Wakeup Reset will not affect RAM or I/Os (See FIG.1).

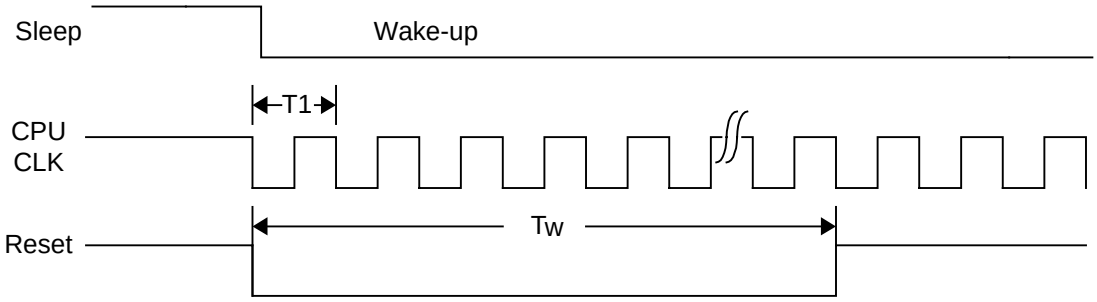
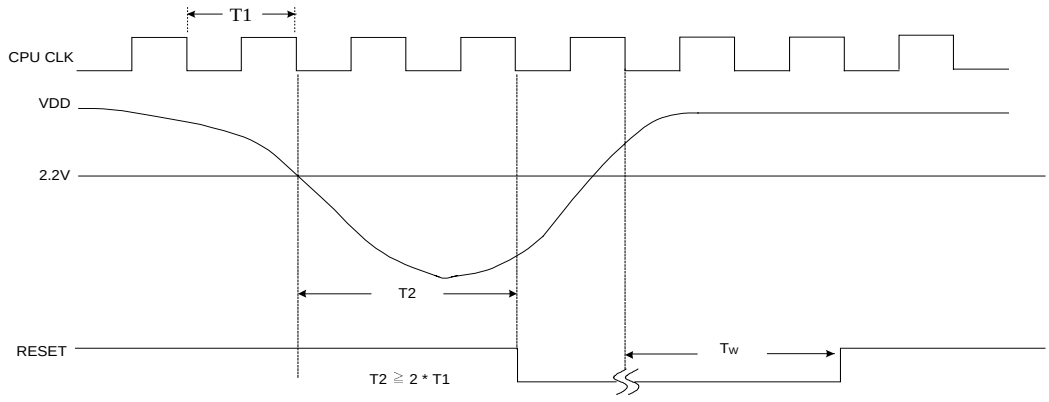


FIG. 1

T1 = 1 / (F_{CPU}), Tw ≧65536 x T1

■ LOW VOLTAGE RESET

The SPC500A1 provides a Low Voltage Reset (LVR) function. Below the minimum power-supply voltage of 2.2V, the CPU system will become unstable and malfunction. Low Voltage Reset will reset all functions into the initial operational (stable) state if the VDD power-supply voltage drops below 2.2V (See FIG.2).



(The LVR function is the same as Power ON Reset or External Reset.)

FIG. 2

■ TIMER/COUNTER

The SPC500A1 contains two 12-bit timer/counters, TMA and TMB respectively. TMA can be specified as a timer or a counter, but TMB can only be used as a timer. In the timer mode, TMA and TMB are re-loaded up-counters. When timer overflows from $0FFF to $0000, the carry signal will make the timer automatically reload to the user's pre-set value and be up-counted again. At the same time, the carry signal will generate the INT signal if the corresponding bit is enabled in the INT ENABLE Register. If TMA is specified as a counter, users can reset by loading #0 into the counter. After the counter has been activated, the value of the counter can also be read from the counters at the same time.

Clock source of Timer/Counter can be selected as follows:

Timer/Counter		Clock Source
TMA	12-BIT TIMER	CPU CLOCK (T) or T/4
	12-BIT COUNTER	T/64, T/8192, T/65536 or EXT CLK
TMB	12-BIT TIMER	T or T/4
MODE SELECT REGISTER		TMA only, select timer or counter
TIMER CLOCK SELECTOR		Select T or T/4

■ SPEECH AND MELODY

Since the SPC500A1 provides a large ROM and wide range of CPU operation speeds, it is most suitable for speech and melody synthesis. For speech synthesis, the SPC500A1 can provide NMI for accurate sampling frequency. Users can record or synthesize the sound and digitize it into the ROM. The sound data can be played back in the sequence of the control functions as designed by the user's program. Several algorithms are recommended for high fidelity and compression of sound including PCM, LOG PCM, and ADPCM. For melody synthesis, the SPC500A1 provides the dual tone mode. After selecting the dual tone mode, users only need to fill either TMA or TMB, or both TMA and TMB to generate expected frequency for each channel. The hardware will toggle the tone wave automatically without entering into an interrupt service routine. Users are able to simulate musical instruments or sound effects by simply controlling the envelope of tone output.

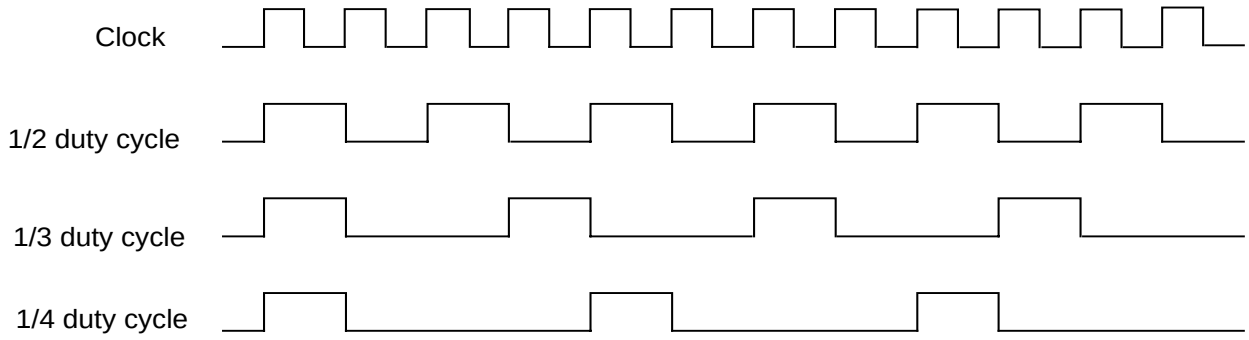
■ SERIAL INTERFACE I/O

The SPC500A1 provides serial interface I/O mode for those applications requiring large ROM/RAM. Serial Interface I/O Port can be used to read/write data from/to extra memory. The interface I/O Register is the control register for programming interface I/O.

■ MULTI-DUTY CYCLE MODE

The SPC500A1 provides three output waveforms, 1/2, 1/3, and 1/4 duty cycles. The Control Register should be used to select 1/2, 1/3 or 1/4 duty cycle and the IOA2 should be programmed as the multi-duty cycle output port. Users can use the combinations of these duty cycles for remote-control purposes.

■ **1/2, 1/3, 1/4 duty cycle outputs**



PIN DESCRIPTIONS*

Mnemonic	PIN No.	Type	Description
VDD	11,15	I	Positive supply for logic and I/O pins
VSS	1,10	I	Ground reference for logic and I/O pins
XI	13	I	Oscillator crystal input or RESISTOR (Resistor should be connected to VDD)
XO	12	O	Oscillator crystal output
TEST	17	I	TEST MODE
RESET	2	I	This pin is an active low reset to the chip
AUD1 AUD2	14 16	O	AUDIO OUTPUT
IOA0 IOA1 IOA2 IOA3	30 31 32 33	I/O I/O I/O I/O	Port A is an 4-bit bi-directional programmable Input / Output port with Pull-high or Open-drain option. As inputs, Port A can be in either the Pure or Pull-high states. As outputs, Port A can be either Buffer or Open-drain NMOS types (Sink current). IOA0: Serial programming clock output IOA2: Multi-duty cycle output **See note 1 and 2 below.
IOB0 IOB1 IOB2 IOB3	26 27 28 29	I/O I/O I/O I/O	Port B is an 4-bit bi-directional programmable Input / Output port with Pull-low or Open-drain option. As inputs, Port B can be in either the Pure or Pull-low states. As outputs, Port B can be either Buffer or Open-drain NMOS types (Sink current). **See note 1 and 2 below.
IOC0 IOC1 IOC2 IOC3 IOC4 IOC5 IOC6	3 4 5 6 7 8 9	I/O I/O I/O I/O I/O I/O I/O	Port C is an 7-bit bi-directional Input / Output port with Pull-high or Open-drain option. As inputs, Port C can be in either the Pure or Pull-high states. As outputs Port C can be a Buffer type or Open-drain NMOS type (sink current). IOC0: Serial programming Data IOC1: Can also be selected as an external interrupt PIN IOC2: EXT COUNT IN **See note 1 and 2 below.

Mnemonic	PIN No.	Type	Description
			Port D is an 8-bit bi-directional programmable Input / Output port with Pull-
IOD0	18	I/O	low or Open-drain option. As inputs, Port D can be either Pure or Pull-low
IOD1	19	I/O	states. As outputs, Port D can be either Buffer or Open-drain PMOS type
IOD2	20	I/O	(send current).
IOD3	21	I/O	(Port D can be software programmed for wake up I/O PIN)
IOD4	22	I/O	(Programmable I/O, Key change, Wake up I/O)
IOD5	23	I/O	
IOD6	24	I/O	
IOD7	25	I/O	**See note 1 and 2 below.

* Refer to SPC Programming Guide for complete information.

**Note: 1.) Two input states can be specified; Pure Input, Pull-High or Pull Low.

2.) Three output states can be specified, Buffer output, Open Drain PMOS output <send>, Open Drain NMOS output <sink>.

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Ratings
DC Supply Voltage	V+	< 7V
Input Voltage Range	V_{IN}	-0.5V to V+ + 0.5V
Operating Temperature	T_A	0℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

AC CHARACTERISTICS (TA = 25 ℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
CPU Clock	F_{CPU}	-	3.58	5.0	MHz	VDD = 3V
		-	4.0	8.0	MHz	VDD = 5V

DC CHARACTERISTICS (TA = 25 ℃, VDD = 3V)

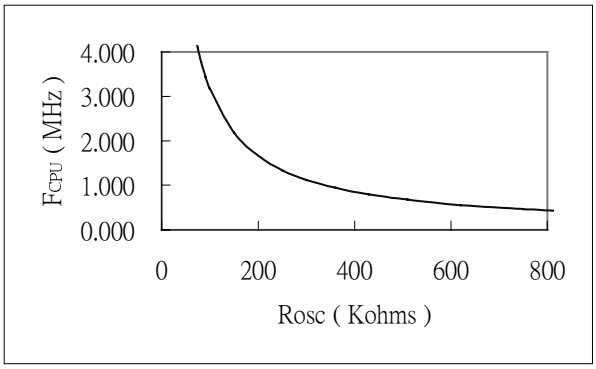
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	V_{DD}	2.4	-	3.4	V	For 2-battery
Operating Current	I_{OP}	-	1.5	2.0	mA	F_{CPU} = 3.0MHz @ 3V, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 3V
Audio output current	I_{AUD}	-	-1.5	-	mA	VDD = 3V, one-channel
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3V
Output High I IOA,IOB,IOC,IOD	I_{OH}	-1.0	-	-	mA	VDD = 3V V_{OH} = 2V
Output Sink I IOA,IOB,IOC,IOD	I_{OL}	2.0	-	-	mA	VDD = 3V V_{OL} = 0.8V
Input Resistor IOB,IOD	R_{IN}	-	100	-	Kohm	Pull Low VDD = 3V

DC CHARACTERISTICS (TA = 25 ℃, VDD = 5V)

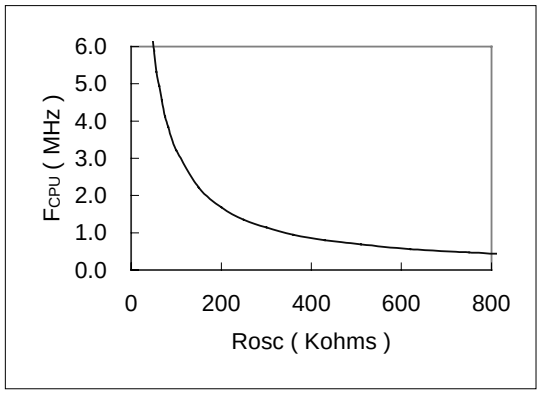
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	V_{DD}	3.6	-	5.5	V	For 3-battery
Operating Current	I_{OP}	-	4.0	5.0	mA	F_{CPU} = 4.0MHz @ 5V, no load
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 5V
Audio output current	I_{AUD}	-	-3.0	-	mA	VDD = 5V, one-channel
Input High Level	V_{IH}	3.0	-	-	V	VDD = 5V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 5V
Output High I IOA,IOB,IOC,IOD	I_{OH}	-1.0	-	-	mA	VDD = 5V V_{OH} = 4.2V
Output Sink I IOA,IOB,IOC,IOD	I_{OL}	4.0	-	-	mA	VDD = 5V V_{OL} = 0.8V
Input Resistor IOB,IOD	R_{IN}	-	70	-	Kohm	Pull Low VDD = 5V

The relationship between the Rosc and the F_{CPU}

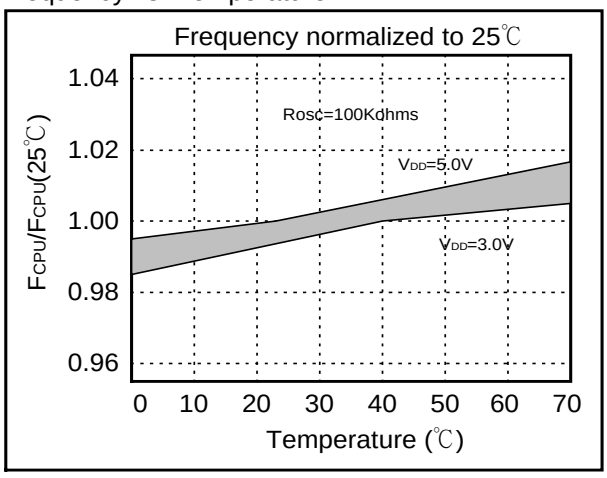
VDD = 3.0V , Ta = 25℃



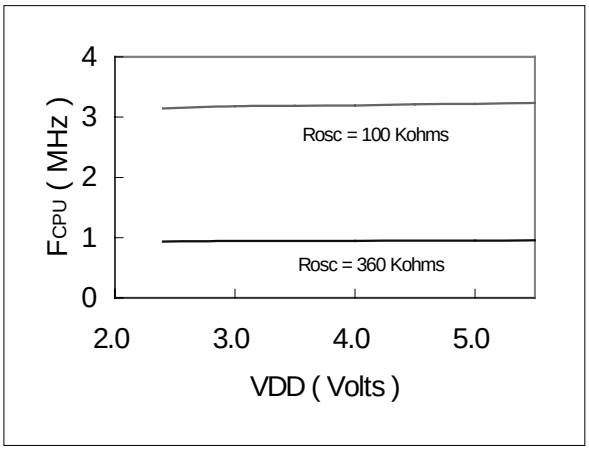
VDD = 5.0V , Ta = 25℃



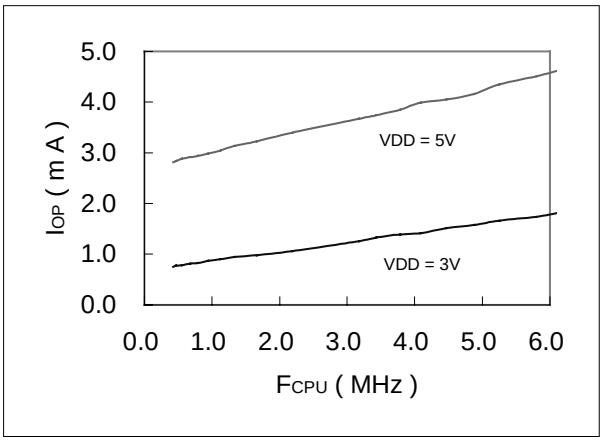
Frequency vs. Temperature



Frequency vs. VDD

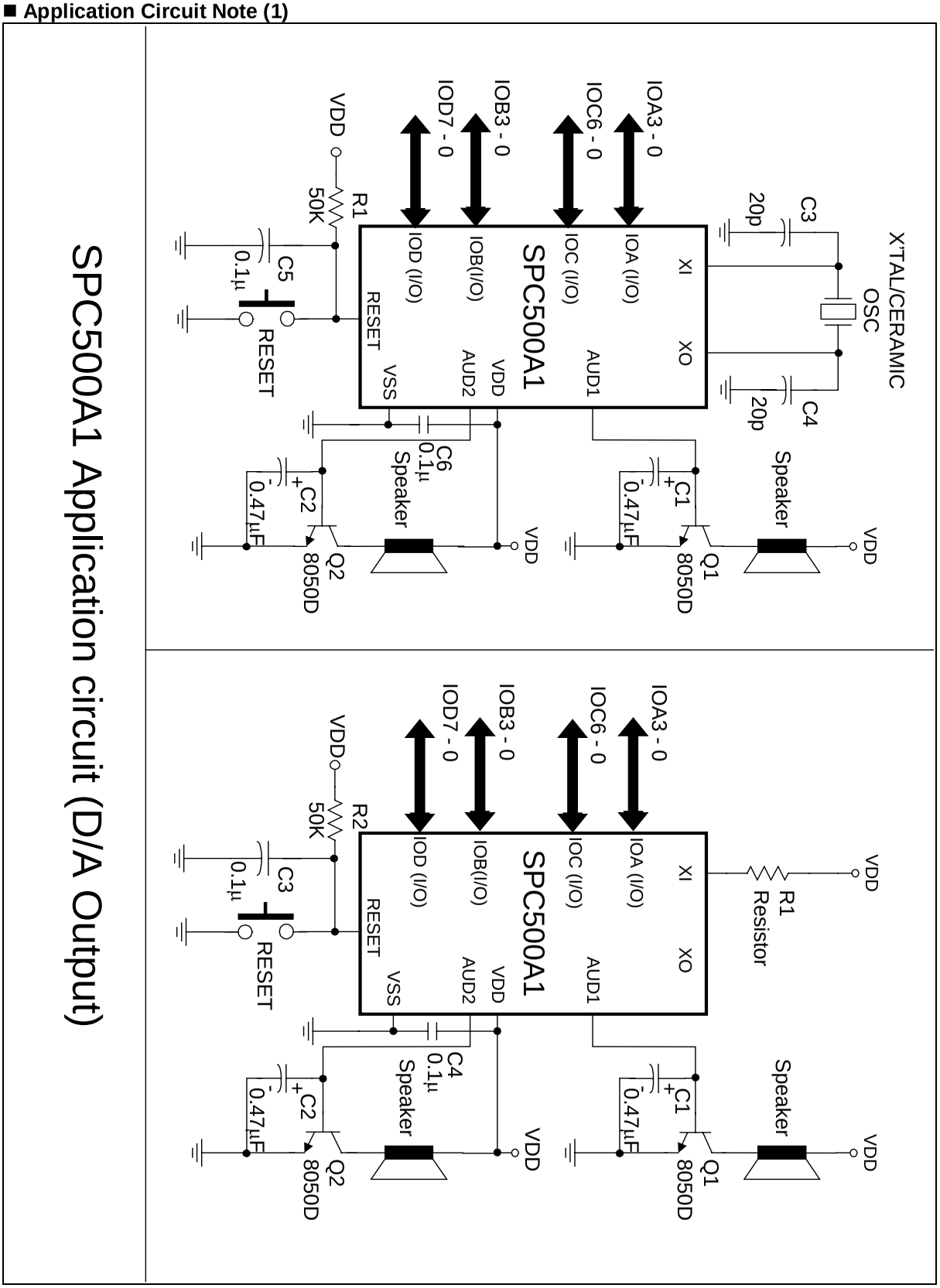


Operating current vs. Frequency vs. VDD

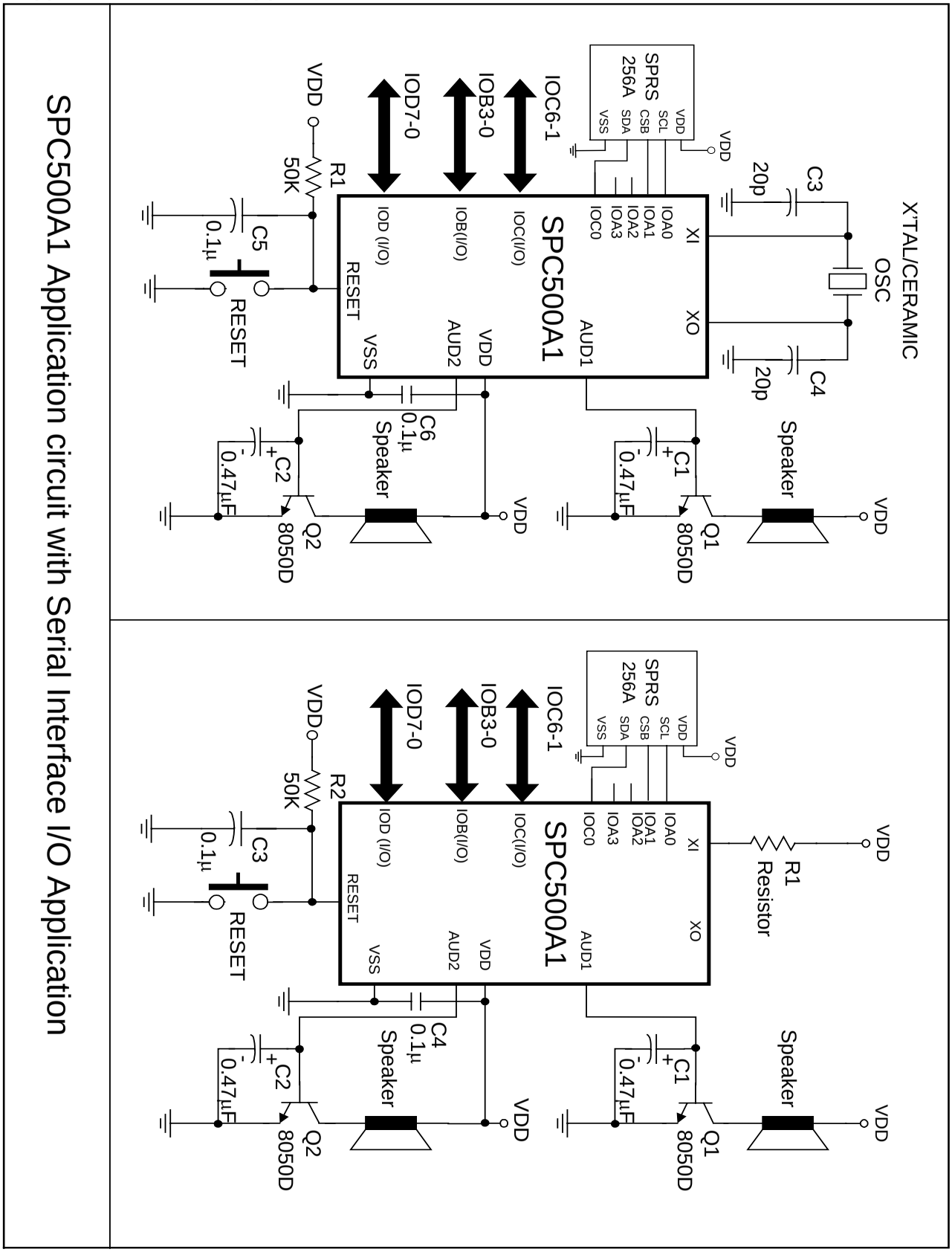


APPLICATION CIRCUIT NOTES

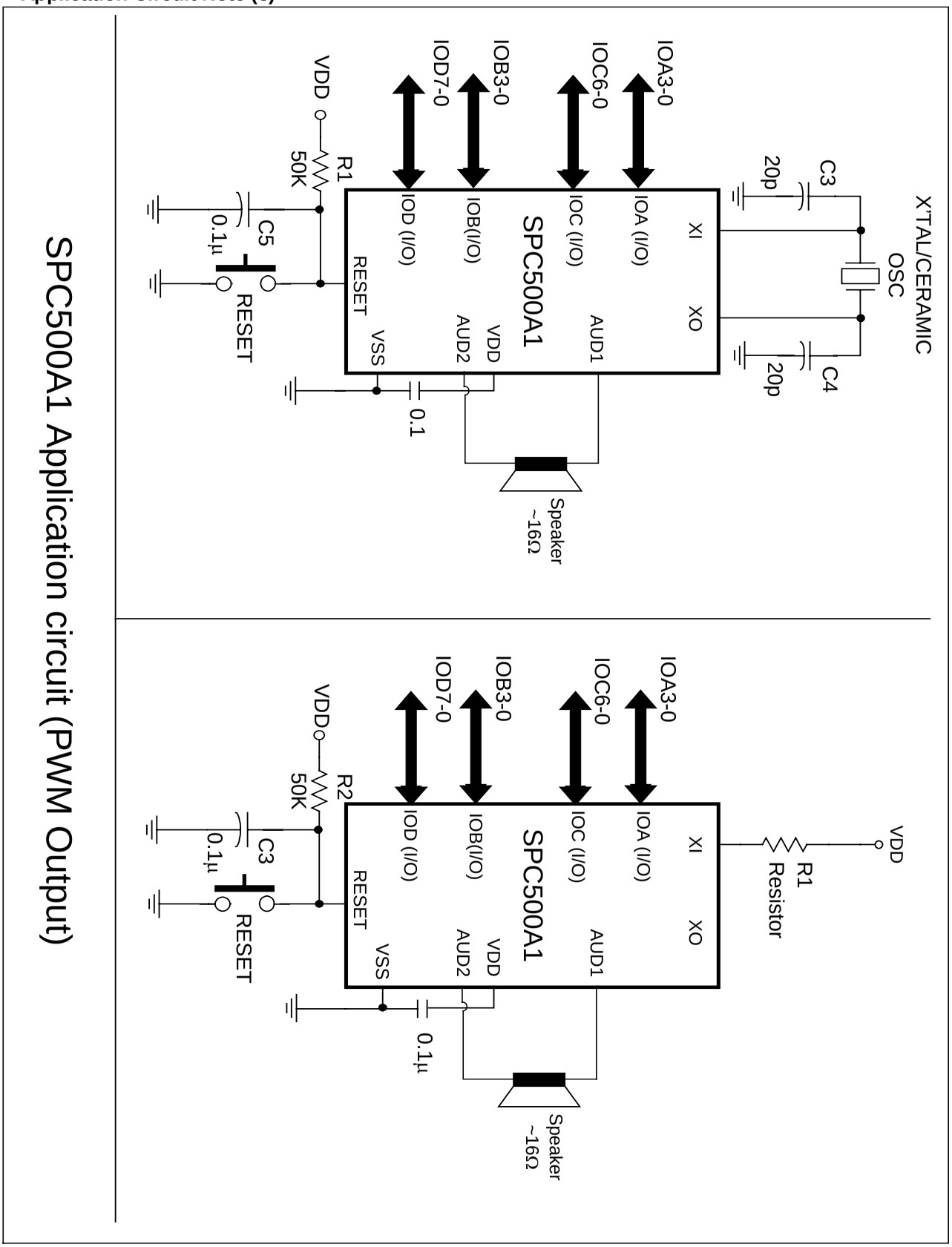
■ **Application Circuit Note (1)**



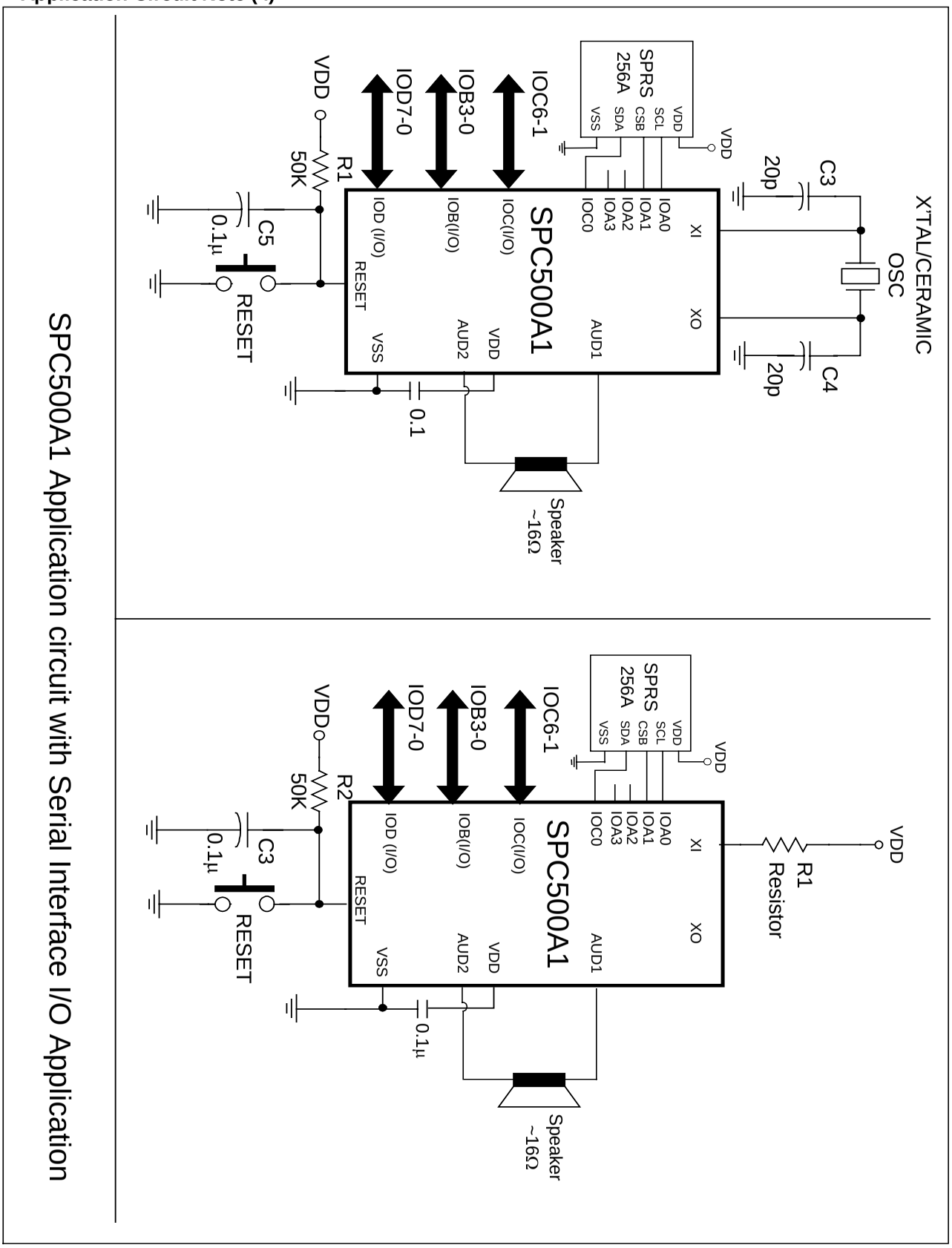
■ **Application Circuit Note (2)**



■ **Application Circuit Note (3)**

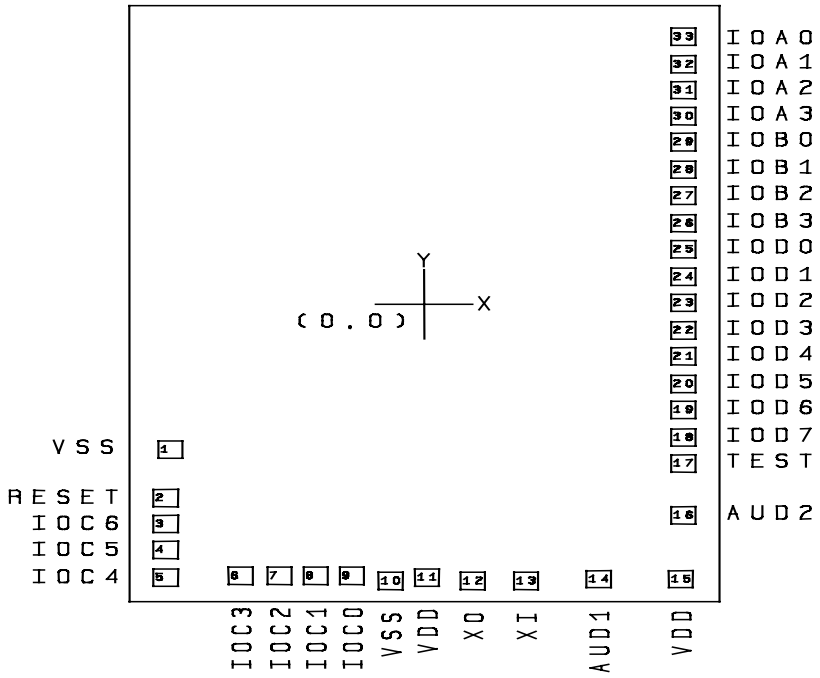


■ **Application Circuit Note (4)**



PAD ASSIGNMENT AND LOCATIONS

■ PAD Assignment



Chip Size: 2550μm x 3380μm

This IC substrate should be connected to VSS

Note: To ensure that the IC functions properly, bond all VDD, VSS, AVDD and AVSS pins.

Ordering Information

Product Number	Package Type
SPC500A1-nnnnV-C	Chip form

Note1: Code number (nnnnV) is assigned for customer.

Note2: Code number (nnnn = 0000 - 9999); version (A = A - Z).

NOTE: SUNPLUS TECHNOLOGY CO., LTD reserves the right to make changes at any time without notice in order to improve the design and performance and to supply the best possible product.

■ **PAD Locations**

Pad No	Pad Name	X	Y
1	VSS	-1116	-1041
2	RESET	-1130	-1317
3	IOC6	-1130	-1473
4	IOC5	-1130	-1624
5	IOC4	-1130	-1779
6	IOC3	-814	-1774
7	IOC2	-659	-1774
8	IOC1	-507	-1774
9	IOC0	-352	-1774
10	VSS	-201	-1802
11	VDD	-51	-1743
12	XO	144	-1802
13	XI	361	-1802
14	AUD1	663	-1781
15	VDD	1090	-1791
16	AUD2	1063	-1457
17	TEST	1121	-1174
18	IOD7	1121	-1023
19	IOD6	1121	-864
20	IOD5	1121	-713
21	IOD4	1121	-555
22	IOD3	1121	-403
23	IOD2	1121	-245
24	IOD1	1121	-93
25	IOD0	1121	65
26	IOB3	1121	217
27	IOB2	1121	375
28	IOB1	1121	527
29	IOB0	1121	685
30	IOA3	1121	836
31	IOA2	1121	992
32	IOA1	1121	1143
33	IOA0	1121	1298

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